Revision Guide for A-Level Computer Science Unit 1.1.1 (SLR 01)

1.1.1 Structure and function of the processor

Candidates need to have an understanding of the purpose and function of the core components of a processor	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆
Candidates need to understand the role and components of the ALU.	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆
Candidates need to understand the purpose and function or registers within the processor, including the PC, accumulator, MAR, MDR and CIR	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆
Candidates need to understand the purpose, function and role of the data, address and control buses in the processor.	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆
Candidates need to understand how assembly language makes use of registers, and how data and addressed are transferred between registers.	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆
Candidates need to understand the purpose and stages within the FDE cycle	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆
Candidates need to understand how and when the registers are used within this cycle, and how and where data and addresses are transmitted to/from in each part of this cycle.	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆
Candidates need to understand how the performance of the CPU can be affected by many factors.	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆
Candidates need to understand how and why the performance is affected by the clock speed, the number of cores and the size and speed of the cache.	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆
Candidates need to have an understanding of the Von Neumann and Harvard architectures. They should be aware of the different approaches the architectures take to storing instructions and data in memory and the benefits of each approach.	Before Revision☆☆☆☆☆ After Revision☆☆☆☆☆

Slideshow (Shared area)	PG Online Textbook	Teach-ICT	CraignDave (Youtube)
Slides 1 to 91 **Read ☐** **Starter Activities ☐** **Activities ☐** **Questions ☐**	Section 1: Chapters 1 & 3 Pages 2 to 11 **Read ☐** **Questions ☐** **Exercises P6 & P9 ☐**	1.1.1 Architecture – Main parts of a CPU **Theory ☐** **Lesson Tasks ☐** 1.1.1 Architecture – Registers within the CPU **Theory ☐** **Lesson Tasks ☐** 1.1.1 Architecture – Fetch – Decode - Execute Cycle **Theory ☐** **Lesson Tasks ☐** 1.1.1 Architecture – CPU Performance factors **Theory ☐** **Lesson Tasks ☐** 1.1.1 Architecture – von Neumann and Harvard **Video ☐** **Theory ☐** **Lesson Tasks ☐**	OCR A'Level ALU, CU, Registers and Buses **Watched ☐** **Cornell Notes ☐** OCR A'Level Fetch decode execute cycle **Watched ☐** **Cornell Notes ☐** OCR A'Level Performance of the CPU **Watched ☐** OCR A'Level Pipelining **Watched ☐** **Cornell Notes ☐** OCR A'Level von Neumann and Harvard **Watched ☐** **Cornell Notes ☐**

Also access to previous notes from GCSE and GCSE resources can be located in the student resources (shared area)